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# PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): 550-228

**FACSIMILE CERTIFICATE**

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Signature: _____

Typed or printed name: Stanley C. Spooner

| Application Number | Filed |
|---|---|
| 09/845,329 | May 1, 2001 |

First Named Inventor: MARTIN SAN JUAN

| Art Unit | Examiner |
|---|---|
| 2662 | H. Cho |

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ Applicant/Inventor

☐ Assignee of record of the entire interest. See 37 C.F.R. § 3.71. Statement under 37 C.F.R. § 3.73(b) is enclosed. (Form PTO/SB/96)

☒ Attorney or agent of record 27,393 (Reg. No.)

☐ Attorney or agent acting under 37CFR 1.34.
Registration number if acting under 37 C.F.R. § 1.34 _____

Signature

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Typed or printed name

703-816-4028
Requester's telephone number

November 8, 2005
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.*

☒ *Total of 1 form/s are submitted.



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**STATEMENT OF ARGUMENTS IN SUPPORT OF PRE-APPEAL BRIEF REQUEST FOR REVIEW**

The following listing of clear errors in the Examiner's second non-final Official Action are responsive to the Official Action mailed August 8, 2005 (Paper No. 08032005) and are set out in the order that these errors exist in the rejection. The Examiner's allowance of claims 3-8 and 10 is very much appreciated.

**1. No prior art reference teaches Applicant's claimed "second bus for coupling a second master logic unit with a subset of said plurality of slave logic units"**

The Court of Appeals for the Federal Circuit has noted in the case of *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick*, 221 USPQ 481, 485 (Fed. Cir. 1984) that "[a]nticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Claim 1 specifies "a second bus for coupling a second master logic unit with a subset of said plurality of slave logic units." Therefore, in order to anticipate, Yanai must contain a teaching of a bus for coupling a logic unit to "a **subset** of said plurality of slave logic units." (emphasis added).

The Examiner alleges that Yanai teaches every element set out in Applicant's independent claim 1. However, the Examiner has not demonstrated how or where the Yanai reference contains any teaching of a second bus for coupling a second master logic unit with a "subset of said plurality of slave logic units." In fact, a review of Yanai's Figure 1 (using the Examiner's analogy that the A and B buses are the claimed first and second bus) it can be seen that each bus connects its respective master logic unit with **both** resources 16 and 18. Thus, there is clearly no teaching of connection with a subset of units and in fact Yanai specifically suggests

interconnecting, not with the subset, but with all of the slave logic units in both the first and second buses.

Yanai clearly fails to disclose the structure of the "second bus" set out in Applicant's independent claim 1 and therefore the rejection of claim 1 and claims 2 and 11 dependent thereon is unwarranted.

**2. No prior art reference teaches a "slave interface mechanism . . . to connect either the first bus or the second bus"**

Applicant's independent claim 1 also specifies a "slave interface mechanism associated with each slave logic unit in said subset and comprising switching logic arranged to **connect either the first bus or the second bus** to the corresponding slave logic unit . . . ." (emphasis added). Thus, the slave interface connects slave logic units "in said subset" to "either the first bus or the second bus."

The Examiner again fails to point out any teaching in the Yanai reference in which the slave logic units are connected to "either the first bus or the second bus." In fact, while the Examiner suggests that the Yanai "abstract" supports his interpretation (that Yanai somehow teaches the claimed "slave interface mechanism"), the abstract actually teaches the direct opposite. Note the Yanai abstract specifically states that the arbitrators allow "first and second computer system devices **to access first and second computer system resources simultaneously**." (Emphasis added). In other words, Yanai clearly teaches simultaneous connection rather than the claimed "either the first bus or the second bus."

Thus, Yanai clearly fails to disclose the "slave interface mechanism" set out in Applicant's independent claim and therefore the rejection of claims 1, 2 and 11 under 35 USC §102 clearly fails.

**3. The Examiner has failed to identify any "reason" or "motivation" for combining elements of the Yanai and Lai references**

In rejecting claim 9 as allegedly being obvious over the combination of Yanai and Lai, the burden is on the Examiner to provide some reason or motivation for combining the references. The Court of Appeals for the Federal Circuit has held in the case of In re Rouffet, 47 USPQ2d 1453, 1457-8 (Fed. Cir. 1998) that

> to prevent the use of hindsight based on the invention to defeat patentability of the invention, **this court requires the examiner** to show a motivation to combine the references that create the case of obviousness. In other words, **the Examiner must show reasons** that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed." (emphasis added).

In the paragraph bridging pages 3 and 4 of the Official Action, the Examiner provides only a conclusory sentence suggesting that it would be obvious to combine Yanai with Lai, but fails to provide the required "reason" or "motivation" for such a combination.

There is no indication by the Examiner that either Yanai or Lai are directed to solving the problems which are solved by the present invention, i.e., the limitation on the speed of operation of the master logic units being granted access to a bus (see Applicant's specification, page 2, lines 14-19). Not only is there no reason or motivation in Yanai and Lai, the Examiner has not even alleged there to be any motivation.

"The PTO has the burden under §103 to establish a *prima facie* case of obviousness." *In re Fine*, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). The Examiner has failed to meet his burden under 35 USC §103 and any further rejection of claim 9 is respectfully traversed.

**4. Yanai, by suggesting connection to bus lines "simultaneously," teaches away from the claimed connection of "either the first bus or the second bus"**

The Court of Appeals for the Federal Circuit has clearly held that it is "error to find obviousness where references 'diverge from and teach away from the invention at hand'." *In re Fine*, at 1599.

As noted above in section 2, Yanai not only fails to teach a "subset" being coupled by the second bus, but it also fails to teach a slave mechanism connecting "either the first bus or the second bus." In each instance, Yanai teaches the direct opposite of Applicant's claim 1 language, i.e., the second master logic unit is connected with all of the slave logic units and not a "subset" of the slave logic units and, what the Examiner alleges is the "slave interface mechanism" (requiring connection of "either the first bus or the second bus") is specifically described in the Yanai abstract as providing access "simultaneously."

In each of the above instances, the Yanai reference specifically leads one of ordinary skill in the art away from Applicant's claimed combination. Accordingly, any further rejection of claim 9 under the provisions of 35 USC §103 is respectfully traversed.

**SUMMARY**

The above establish that no prior art reference teaches the recited claim limitations of either "a **subset** of said plurality of slave logic units" or connecting "**either** the first bus **or** the second bus" to the slave logic units. The lack of these claimed elements and interrelationships clearly avoids the rejection of claims 1, 2 and 11 under 35 USC §103. The fact that the Examiner has failed to provide any "reason" or "motivation" for combining the Yanai and Lai references, as well as the fact that Yanai teaches away from the subject matter of claim 1, clearly avoids any basis for rejection of claim 9 under 35 USC §103.

MARTIN SAN JUAN
Appl. No. 09/845,329
November 8, 2005

Applicant respectfully requests that the Pre-Appeal Panel find that the application is allowed on the existing claims and prosecution should be closed.

Respectfully submitted,

NIXON & VANDERHYE P.C.

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**CERTIFICATION OF FACSIMILE TRANSMISSION**

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